AN3250
Application note

M24LR64-R
Multi-bank reference design description and settings

1 Introduction

The M24LR64-R multi-bank reference design has been created to help users increase the memory density of their Dual Interface EEPROM, and has been designed in a way that will minimize the antenna size and the I²C interface footprint on the PCB.

STMicroelectronics has prepared two reference designs:

- ANT4-M24LR-A is a 2-bank reference design with a 128-Kbit EEPROM user memory
- ANT5-M24LR-A is a 4-bank reference design with a 256-Kbit EEPROM user memory

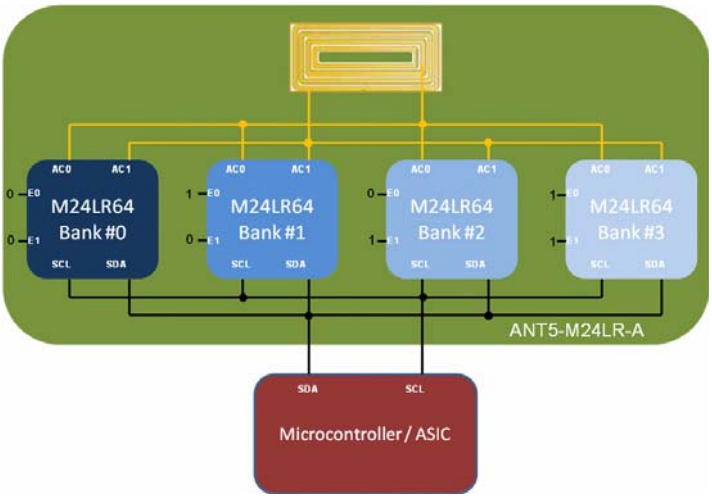
Figure 1. ANT4-M24LR-A design

Figure 2. ANT5-M24LR-A design

The basic principle is to connect several M24LR64-R devices in parallel on the same I²C bus (in compliance with I²C specifications) and for them to share one single antenna.

This application note describes how the M24LR64-R Multi-Bank reference design works from the schematics and design perspective, and explains how to configure and use it.

Figure 3. Design overview



Contents

1 **Introduction** 1

2 **Designing an M24LR64-R multi-bank application** 3

2.1 Accessing several EEPROMs on the same I2C bus 3

2.2 Connecting several M24LR64-R devices on the same inductive antenna . 5

3 **Setting up a Multi-Bank application** 8

3.1 Basic principle 8

3.1.1 Microcontroller's perspective 9

3.1.2 RF reader's perspective 10

3.1.3 Overall perspective 11

3.2 Setting up the Multi-Bank design 12

3.2.1 Microcontroller only is available during setup 12

3.2.2 RFID reader only is available during setup 13

3.2.3 Both Microcontroller and RFID reader are available during setup 14

4 **Conclusion** 15

5 **Revision history** 15

2 Designing an M24LR64-R multi-bank application

2.1 Accessing several EEPROMs on the same I²C bus

The I²C specification allows the use of several devices on the same I²C bus, and this reference design follows this specification. Please refer to the I²C specification and to the M24LR64-R datasheet for more details.

Each device is accessed according to its value defined by the Device Select code.

Table 1. Device Select code description

	Device type identifier(1)				Chip Enable address(2)			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Device Select code	1	0	1	0	E2(3)	E1	E0	RW

1. The most significant bit (b7) is sent first.
2. E0 and E1 are compared against the respective external pins on the memory device.
3. E2 is not connected to any external pin. It is however used to address the M24LR64-R system area as described in the datasheet.

The M24LR64-R offers two Chip Enable pins, E0 and E1. These signals are used to set the values that are to be looked for on bits b2 and b1 of the 7-bit Device Select code.

Figure 4. Logic diagram

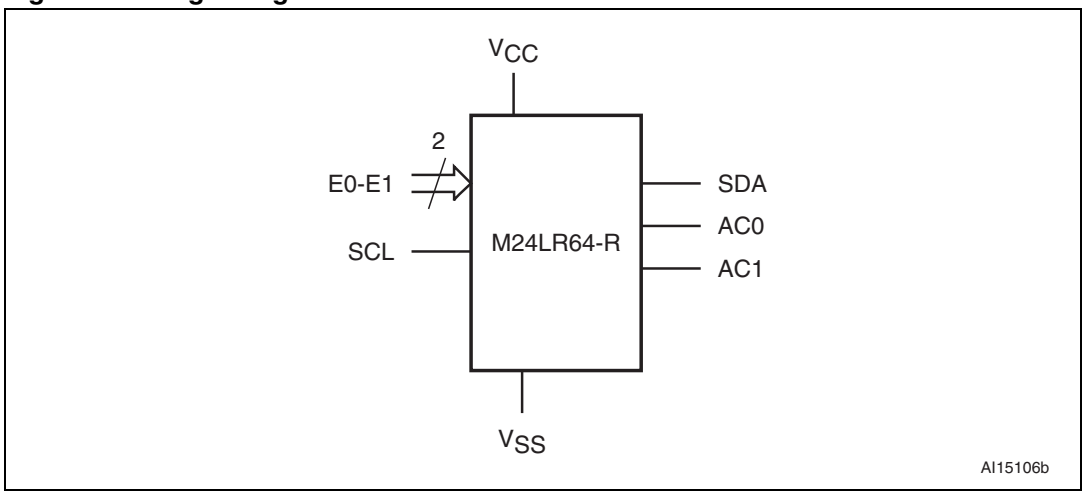


Table 2. Signal descriptions

Signal name	Function	Direction
E0, E1	Chip Enable	Input
SDA	Serial Data	I/O
SCL	Serial Clock	Input
AC0, AC1	Antenna coils	I/O

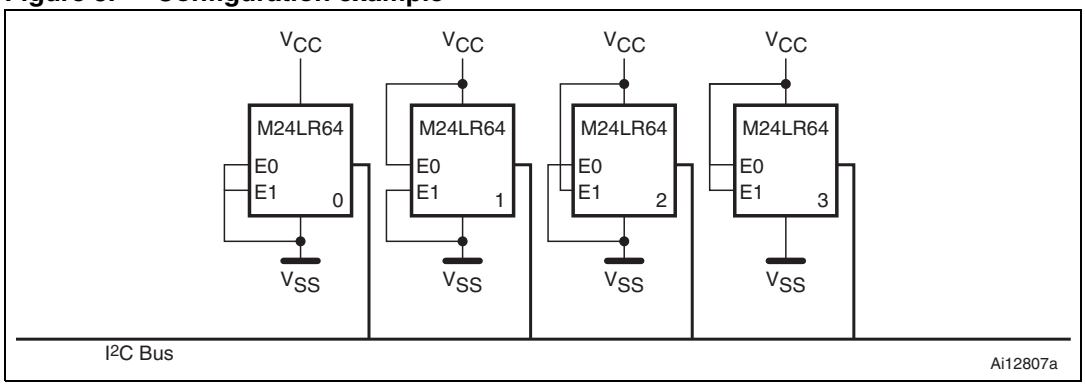
Table 2. Signal descriptions (continued)

Signal name	Function	Direction
V_{CC}	Supply voltage	
V_{SS}	Ground	

E0 and E1 inputs must be tied to V_{CC} (‘1’) or V_{SS} (‘0’) to establish the Device Select code. When not connected (left floating), these inputs are read as low (‘0’). Using bits E0 and E1 of the Device Select code, up to four M24LR64-R devices can be accessed on the same I^2C bus. This enables emulation of up to 256 Kbits of EEPROM.

In the configuration example shown in *Figure 5*, in order to access 256 Kbits of EEPROM, four 64-Kbit M24LR64-R devices are connected to the same I^2C bus and the E0 and E1 signals of each device are assigned in a way to create an unique I^2C address for each specific device.

Figure 5. Configuration example



M24LR64-R #0 (Bank 0)

Device addressed as (**0**,**0**): pin E0 connected to V_{SS} and pin E1 connected to V_{SS}.

	Device type identifier				Chip Enable address			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Device Select code	1	0	1	0	E2	**0**	**0**	RW

M24LR64-R #1 (Bank 1)

Device addressed as (**0**,**1**): pin E0 connected to V_{CC} and pin E1 connected to V_{SS}.

	Device type identifier				Chip Enable address			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Device Select code	1	0	1	0	E2	**0**	**1**	RW

M24LR64-R #2 (Bank 2)

Device addressed as (**1**,**0**): pin E0 connected to V_{SS} and pin E1 connected to V_{CC}.

	Device type identifier				Chip Enable address			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Device Select code	1	0	1	0	E2	**1**	**0**	RW

M24LR64-R #3 (Bank 3)

Device addressed as (**1**,**1**): pin E0 connected to V_{CC} and pin E1 connected to V_{CC}.

	Device type identifier				Chip Enable address			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Device Select code	1	0	1	0	E2	**1**	**1**	RW

To emulate a 256-Kbit device using four M24LR64-R devices, the 256 Kbits are dispatched as follows:

- M24LR64 #0 will store the 1st block of 64-Kbit EEPROM memory area.
- M24LR64 #1 will store the 2nd block of 64-Kbit EEPROM memory area.
- M24LR64 #2 will store the 3rd block of 64-Kbit EEPROM memory area.
- M24LR64 #3 will store the 4th block of 64-Kbit EEPROM memory area.

2.2 Connecting several M24LR64-R devices on the same inductive antenna

The RF interface of M24LR64 devices is based on a passive RFID technology operating at 13.56 MHz in compliance with ISO/IEC 15693 standards. The basic principles of this RF technology and antenna design considerations are described in the following two application notes:

- AN2972: *Designing an antenna for the M24LR64-R dual interface I²C/RFID device*
- AN3178: *Using a surface mount inductor as an M24LRxx antenna*

The basic principle of the M24LR64-R's antenna is very simple; the external antenna inductance ($L_{INDUCTOR}$) that must be integrated on the PCB should match the M24LRxx's internal tuning capacitance (C_{TUNING_IC}) in order to create a circuit resonating at 13.56 MHz. This is because ISO/IEC 15693 RFID readers operate in the 13.56 MHz high frequency band.

$$f_{TUNING} = \frac{1}{2\Pi \bullet \sqrt{L_{INDUCTOR} \bullet C_{TUNINGIC}}}$$

In this reference design, we connect a number *n* of M24LR64-R devices in parallel on the same antenna. The resulting equivalent tuning capacitance ($C_{TUNING\_MULTI\text{-}BANK}$) is *n* times the tuning capacitance of a single M24LR64-R.

$$C_{TUNING\_MULTI\text{-}BANK} = n \times C_{TUNING\_IC}$$

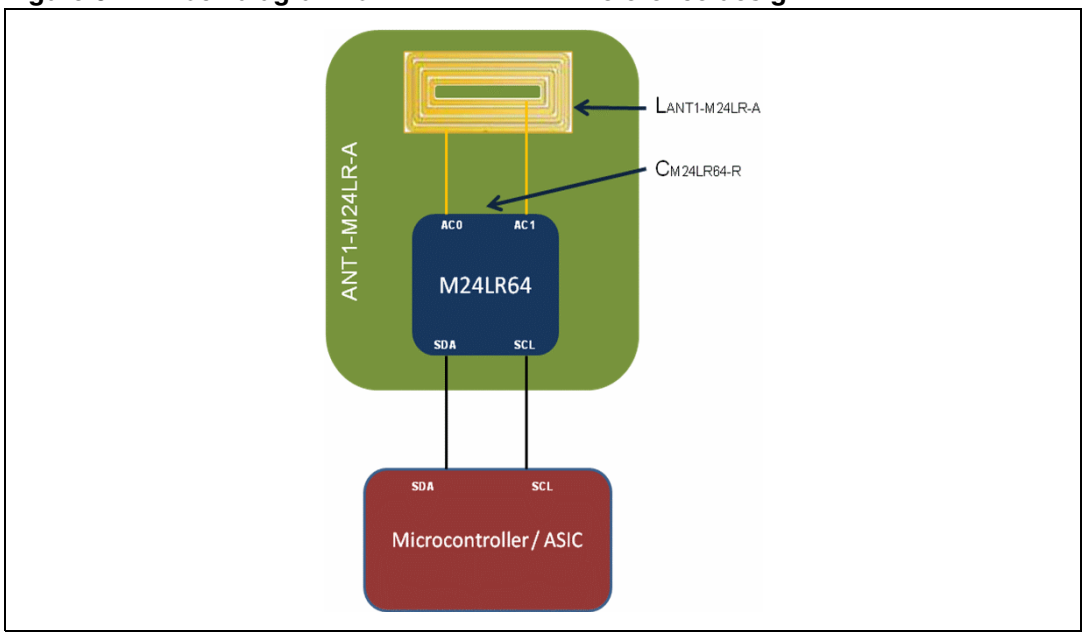
As the antenna tuning frequency (f_{TUNING}) must remain at 13.56 MHz, designers must decrease the antenna inductance by the same factor as the increase of the tuning capacitance of a multi-bank circuit:

$$L_{MULTI\_BANK} = L_{INDUCTOR} / n$$

In the following example, four M24LR64-R devices are connected in parallel on the same antenna. The inductance value of this antenna must be four times smaller than the one used for a single M24LR64-R.

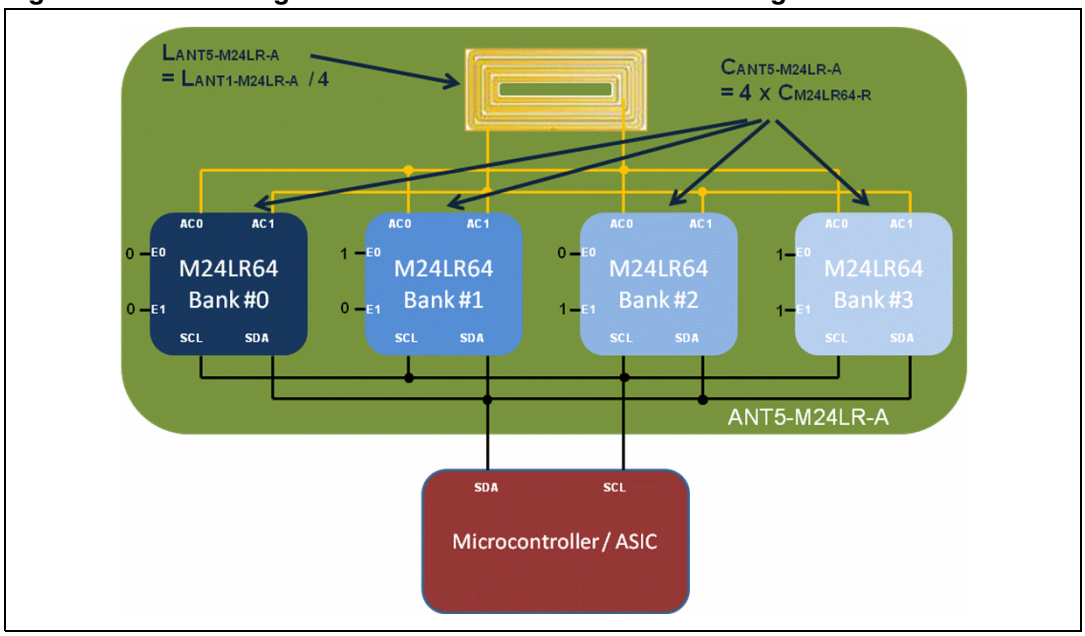
As a reference, *Figure 6* represents a single antenna single M24LR64-R device as per STMicroelectronics ANT1-M24LR-A reference design.

Figure 6. Block diagram for ANT1-M24LR-A reference design



The ANT5-M24LR-A reference design (*Figure 7*) consists of four M24LR64-R devices in parallel, resulting in 256 Kbits of equivalent user memory. The equivalent tuning capacitance value is 4 times that of a single M24LR64-R device. So the antenna, whether it is designed on a PCB or uses an SMD inductor, must be 4 times smaller than the one used for one single M24LR64-R device.

Figure 7. Block diagram for ANT5-M24LR-A reference design



IMPORTANT: As per application notes AN2972 and AN3178, ST recommends antenna designers to prototype different types of antennas with different inductance values in order to select the antenna that will give the best results in their application.

3 Setting up a Multi-Bank application

Once designed, the Multi-Bank application must be configured and programmed so that it can be used correctly by the microcontroller and the RFID reader. Because several banks are used in parallel, each bank must be individually numbered and this number must be common to both the RFID reader and the microcontroller.

This reference design proposes to identify the banks and their numbers using a pointer area placed at the end of the last bank of the reference design.

There are different ways to allocate the banks depending on whether a microcontroller only, an RFID reader only or both a microcontroller and an RFID reader are available in the application during Multi-Bank programming.

For further details on how the M24LR64-R arbitration unit operates, refer to application note AN3057 "*How to manage M24LR64-R data transfers from the I²C bus or an RF channel*".

While the 3 following setup methods work, the one with both a microcontroller and RFID reader is recommend as it speeds up the identification process when the application is running.

3.1 Basic principle

Each memory bank of the Multi-Bank reference design consists of an M24LR64-R memory plan which includes among others:

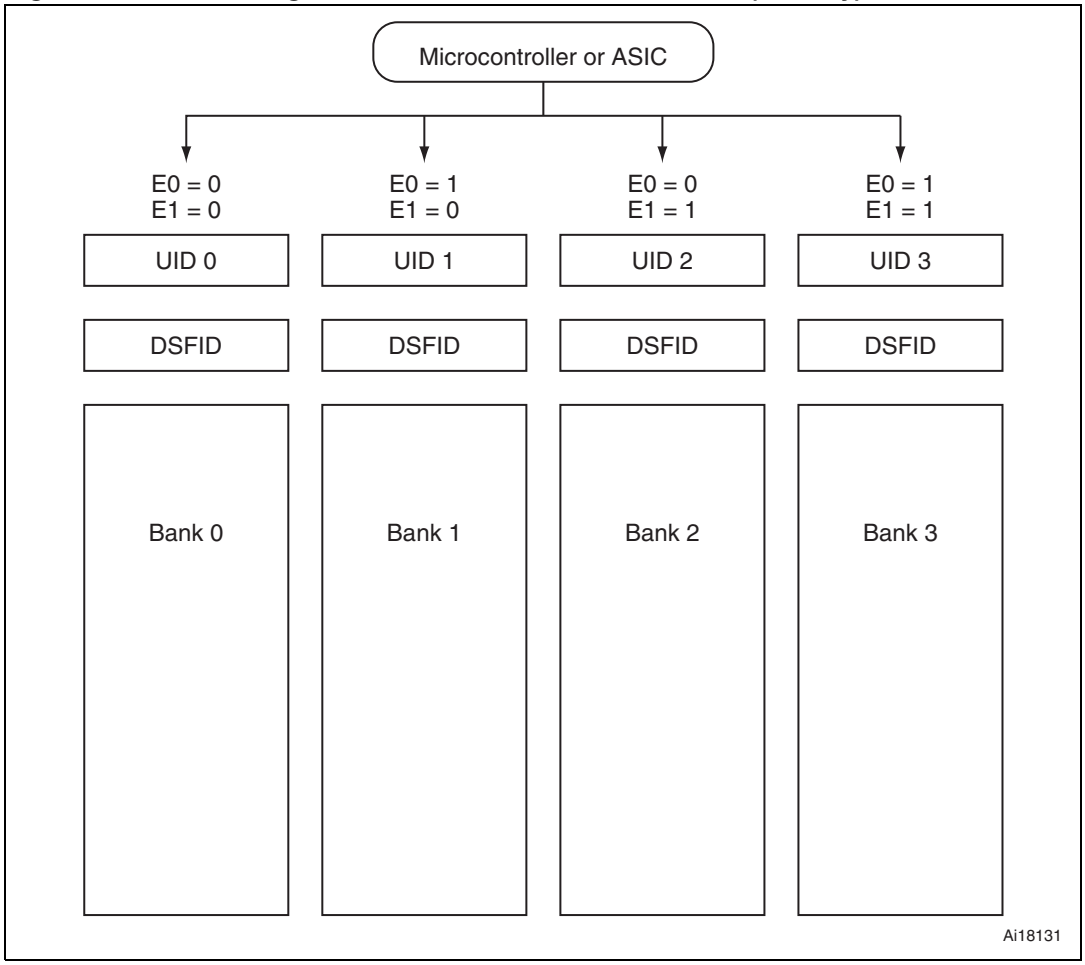
- A 64-bit Unique IDentifier area (UID)
  - Read-only in RF mode
  - Read-only in I^2C mode
- An 8-bit Data Storage IDentifier area (DSFID)
  - Read-write in RF mode
  - Read-only in I^2C mode
- A 64-Kbit EEPROM user memory area
  - Read-write in RF mode
  - Read-write in I^2C mode

Note: This application note illustrates the setup of the ANT5-M24LR-A, which is the 4-bank reference design. The same principle applies for any Multi-Bank design.

3.1.1 Microcontroller's perspective

From the microcontroller's perspective, each bank is addressed using E0 and E1 pins, as shown in *Figure 8*.

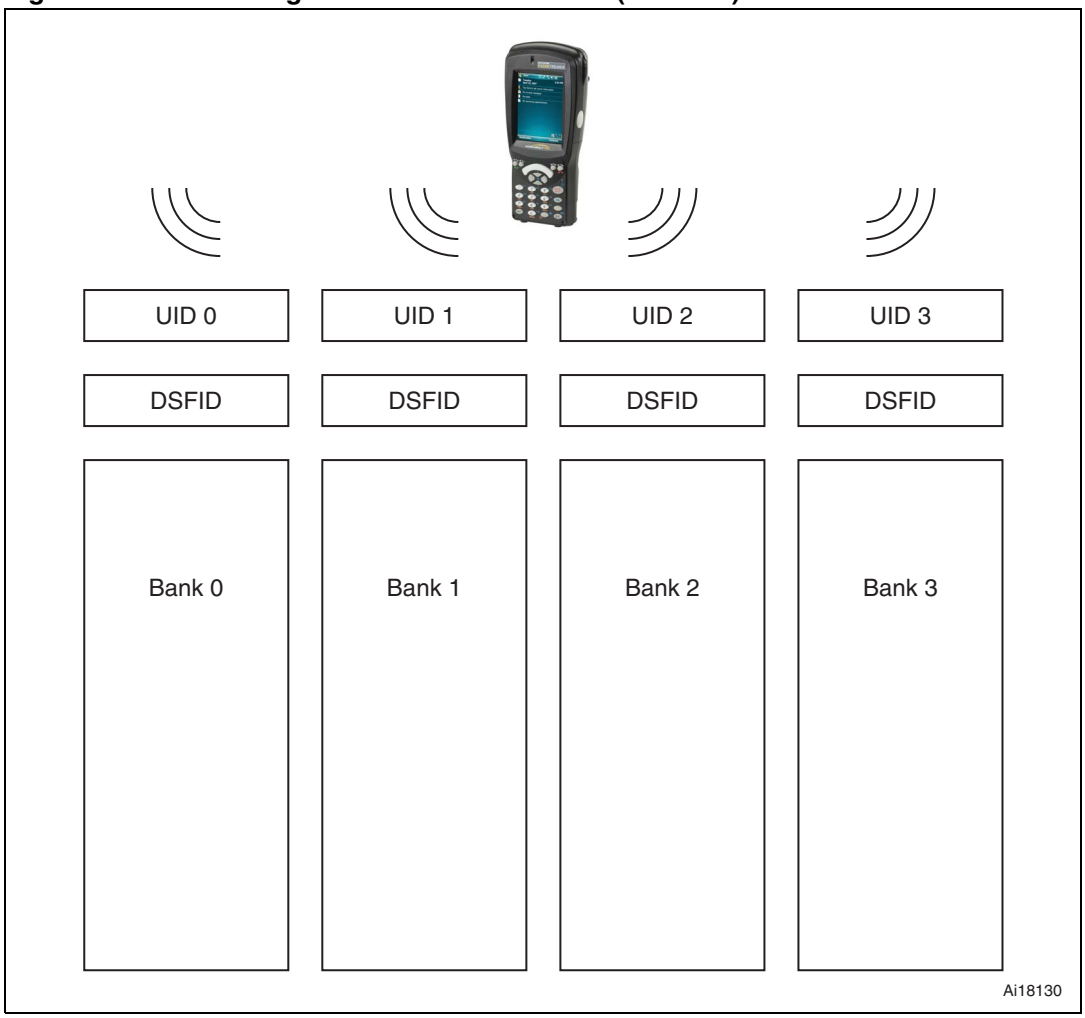
Figure 8. Addressing the 4 banks with a microcontroller (I²C only)



3.1.2 RF reader's perspective

From the RFID reader perspective, each bank is identified by its UID, which is accessible during the basic inventory round. UIDs are used for addressing each device as shown in *Figure 9*.

Figure 9. Addressing the 4 banks in RF mode (with UID)

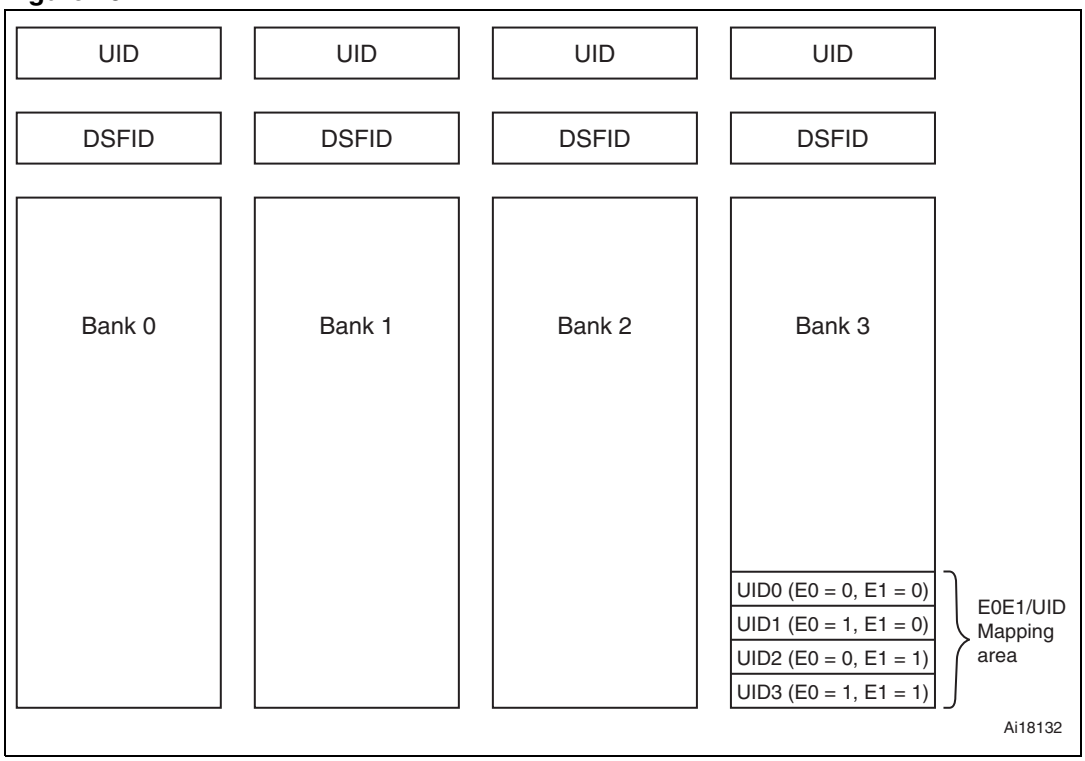


3.1.3 Overall perspective

If both the Microcontroller and the RFID reader need to share the same bank numbering scheme, both E0 E1 values (for addressing each bank by the Microcontroller) and UID values (for addressing each bank by the RFID reader) must be mapped.

This is performed by storing the UID of the corresponding E0E1 signals at the end of the last memory bank as shown in *Figure 10*.

Figure 10.



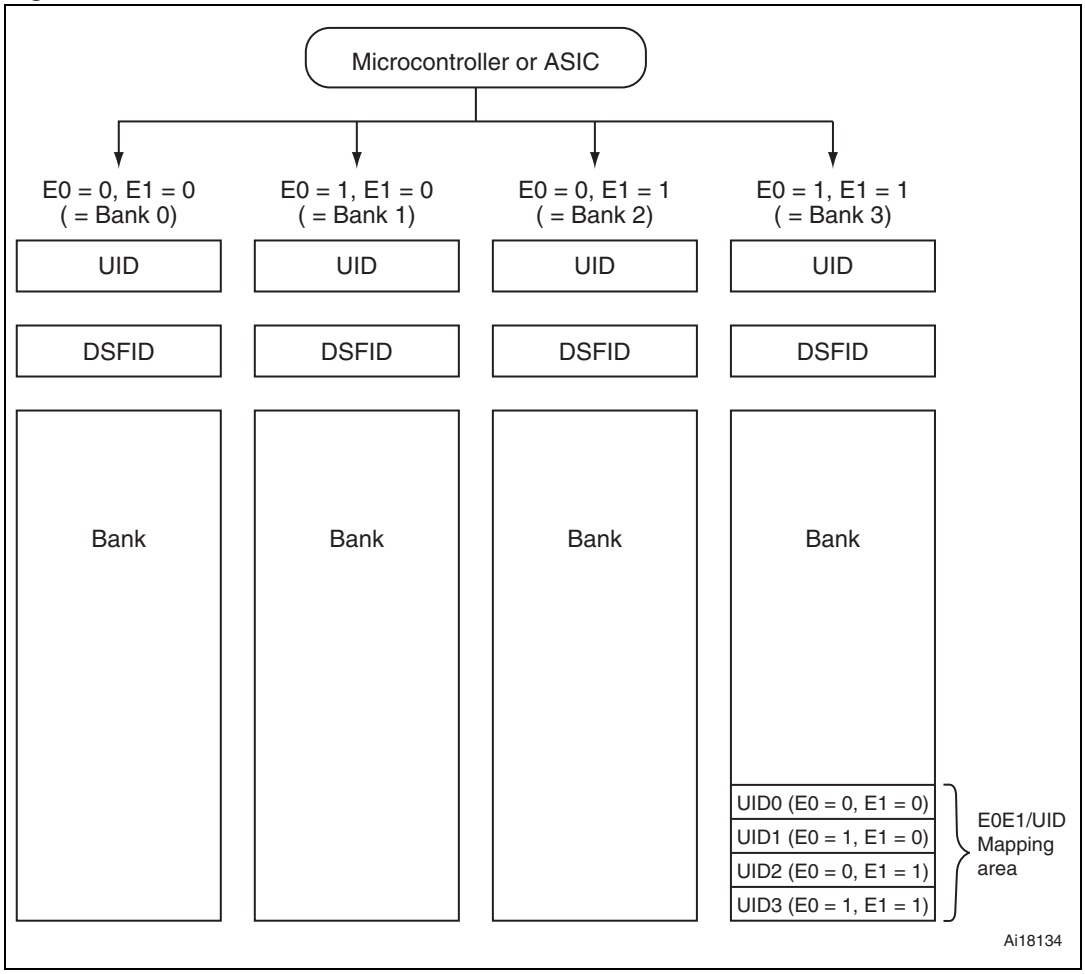
3.2 Setting up the Multi-Bank design

When setting up a multi-bank design, there are different ways to allocate (identify) the banks depending on whether a microcontroller only, an RFID reader only or both a microcontroller and an RFID reader are available during Multi-Bank programming.

3.2.1 Microcontroller only is available during setup

When only the microcontroller (I²C only) is available to program the Multi-Bank setting information, it addresses each M24LR64-R device separately and stores the corresponding UID in its volatile memory.

Figure 11.


Microcontroller or ASIC
E0 = 0, E1 = 0
(= Bank 0)
E0 = 1, E1 = 0
(= Bank 1)
E0 = 0, E1 = 1
(= Bank 2)
E0 = 1, E1 = 1
(= Bank 3)
UID
DSFID
Bank
UID0 (E0 = 0, E1 = 0)
UID1 (E0 = 1, E1 = 0)
UID2 (E0 = 0, E1 = 1)
UID3 (E0 = 1, E1 = 1)
E0E1/UID Mapping area
Ai18134

Once the UIDs of the 4 devices are read, the Microcontroller programs the 4 UIDs at the end of Bank #3, which is addressed with E0=E1=1.

- Program UID of Bank (E0=0, E1=0) at address 0x07F8 and 0x07F9
- Program UID of Bank (E0=1, E1=0) at address 0x07FA and 0x07FB
- Program UID of Bank (E0=0, E1=1) at address 0x07FC and 0x07FD
- Program UID of Bank (E0=1, E1=1) at address 0x07FE and 0x07FF

At this time, the only way for the RFID reader to correctly identify each bank is to read the E0E1 ↔ UID mapping area. This enables the RFID reader to identify the bank number.

It is recommended to lock the sector to prevent from potential further unwanted information loss.

The drawback of this method is the RFID reader needs to read the memory banks until it gets to the mapping area, which may slow the process down.

3.2.2 RFID reader only is available during setup

In this configuration, only the RFID reader is available to allocate (identify) the banks. Since there is no microcontroller, the use of signals E0 E1 to map the UID numbers is not possible, as only the I^2C master knows the corresponding E0 E1 values.

The following operation is to be performed with an ISO 15693 RFID reader supporting the M24LR64-R device, and by placing only one Multi-Bank card (ANT4-M24LR-A or ANT5-M24LR-A) at a time in the reader's field:

- Perform an RF Inventory round.
- Read the four UIDs (one for each bank).
- Randomly attribute an UID value to each bank.
- Program the DSFID value of each bank as follows:
  - Bank 0 (UID of Bank 0): DSFID = B0h
  - Bank 1 (UID of Bank 1): DSFID = B1h
  - Bank 2 (UID of Bank 2): DSFID = B2h
  - Bank 3 (UID of Bank 3): DSFID = B3h
- Program the mapping area at the end of Bank 3, as the following:
  - Write the Bank 0 UID value at address 0x07F8 and 0x07F9
  - Write the Bank 1 UID value at address 0x07FA and 0x07FB
  - Write the Bank 2 UID value at address 0x07FC and 0x07FD
  - Write the Bank 3 UID value at address 0x07FE and 0x07FF

At this stage, the banks are allocated from the RF perspective. From the microcontroller's perspective, users can access any of the 4 banks using signals E0 E1.

Designers can choose to define a scrambling table (E0E1 ↔ UID) for the Microcontroller to know which bank corresponds to each E0 and E1 signal configuration:

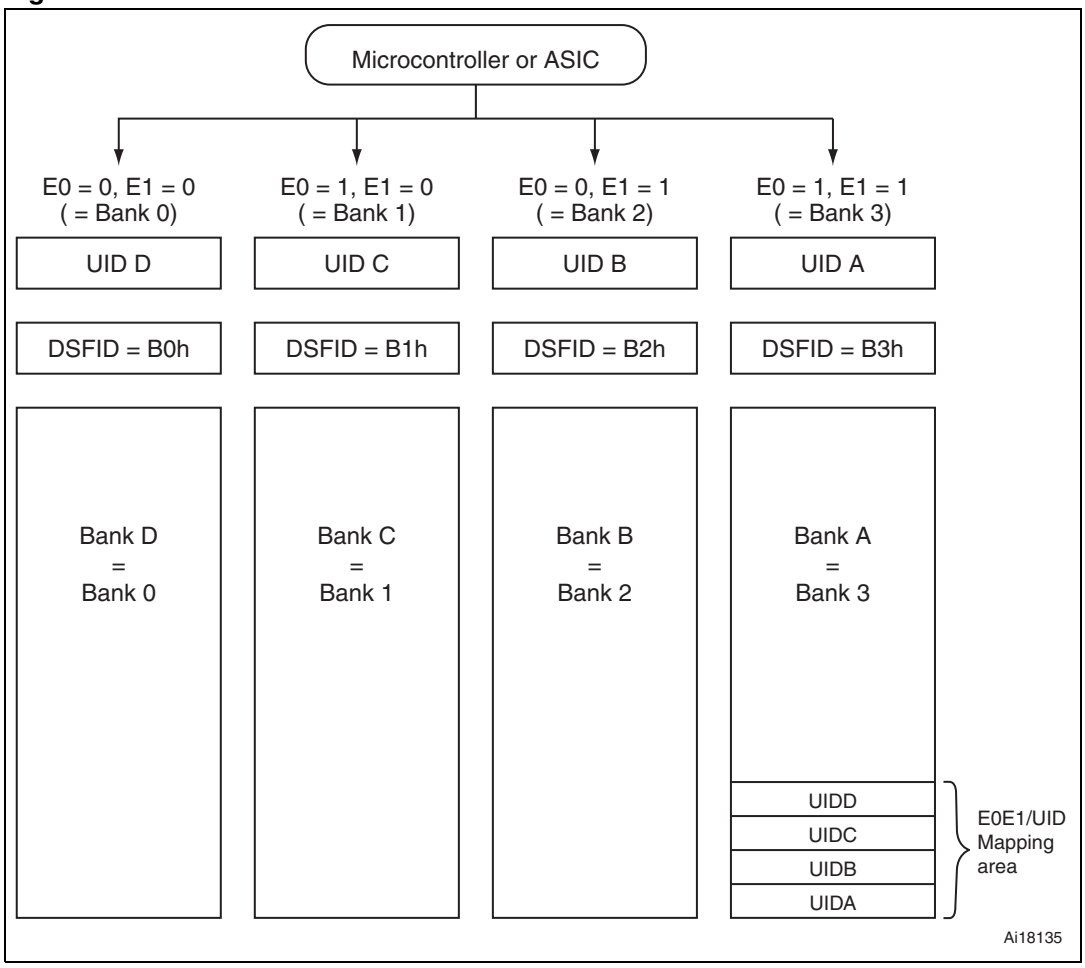
- Read chip @E0E1 = 00b, read DSFID value and map (Bank x ↔ E0E1 = 00b)
- Read chip @E0E1 = 01b, read DSFID value and map (Bank y ↔ E0E1 = 01b)
- Read chip @E0E1 = 10b, read DSFID value and map (Bank z ↔ E0E1 = 10b)
- Read chip @E0E1 = 11b, read DSFID value and map (Bank w ↔ E0E1 = 11b)

3.2.3 Both Microcontroller and RFID reader are available during setup

The setup process starts exactly as in *Section 3.2.1: Microcontroller only is available during setup*.

Once the bank UIDs are programmed in the mapping area, an RF operation can be performed in order to further speed up RF communications by programming the bank UID number stored in the DSFID area. As the DSFID content of each M24LR64-R device (bank) is available during the inventory round, an RFID reader immediately knows with which device it will communicate.

Figure 12.



The following operation is to be performed with an ISO 15693 RFID reader supporting the M24LR64-R device, and by placing only one Multi-Bank card (ANT4-M24LR-A or ANT5-M24LR-A) at a time in the RF reader's field:

- Perform an RF Inventory round.
- Read the last block of each bank until reaching the mapping area.
- Read the UID value for each bank:

```
UID 0 = BANK 0
UID 1 = BANK 1
UID 2 = BANK 2
UID 3 = BANK 3
```

- For each device, write the relevant DSFID value and lock the DSFID:

```
WRITE DSFID B0h (UID0) in addressed mode and lock
WRITE DSFID B1h (UID1) in addressed mode and lock
WRITE DSFID B2h (UID2) in addressed mode and lock
WRITE DSFID B3h (UID3) in addressed mode and lock
```

An example of configuration is available with the M24LR64-R development kit (DEVKIT-M24LR-A).

4 Conclusion

The M24LR64-R multi-bank reference is now ready to use. Other implementations for bank assignment might be more relevant to the user's application.

Users can take advantage of the fact that each bank comes with 3 different passwords each, which gives extra flexibility for data management.

More details are available in application note AN3002 *Description of the M24LR64-R Dual Interface EEPROM's password protection mechanism*.

5 Revision history

Table 3. Document revision history

Date	Revision	Changes
23-Jul-2010	1	Initial release.

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